Journal of Engineering Research and Reports

20(10): 34-38, 2021; Article no.JERR.70393
ISSN: 2582-2926

RSOB Shorting Defect Resolution through Looping Optimization and Ball Placement at Wirebond Process

Norman S. Calma[1], Jonathan C. Pulido[1*] and Frederick Ray I. Gomez[1]

[1]Back-End Manufacturing & Technology, STMicroelectronics, Inc., Calamba City, Laguna, 4027, Philippines.

Authors' contributions

This work was carried out in collaboration among all authors. All authors read, edited and approved the final manuscript.

Article Information

DOI: 10.9734/JERR/2021/v20i1017387
Editor(s):
(1) Dr. Guang Yih Sheu, Chang-Jung Christian University, Taiwan.
Reviewers:
(1) Leyla Taghavifar, Islamic Azad University, Iran.
(2) Ahmad Zaidi Bin Abdullah, UNIMAP, Malaysia.
Complete Peer review History: https://www.sdiarticle4.com/review-history/70393

Original Research Article

Received 04 May 2021
Accepted 09 July 2021
Published 21 July 2021

ABSTRACT

Wirebonding process is one of the most challenging assembly manufacturing process in semiconductor packaging industry. This paper discussed the wirebonding challenge and the solution to resolve the wire to die shorting on reverse stitch on ball (RSOB) and prevent irregular looping height for the substrate land grid array (LGA) device. Comprehensive parameter optimization was done particularly on the wirebond looping to ensure that no wire depression and no capillary hitting would occur wirebonding setup. Ultimately, the optimized wirebonding parameter prevented the occurrence of looping issues during the lot process. For future works, the configuration and technique could be applied on packages with similar situation.

Keywords: Die reference; looping profile; pattern recognition; wirebonding process.

1. INTRODUCTION

Substrate land grid array (LGA) package is commonly used in semiconductor packaging industry due to its high-density input/output (I/O) capability. With continous technology trends and breakthroughs, challenges in assembly manufacturing are expected [1-4]. On top of the

**Corresponding author: Email: jonathan.pulido@st.com;*

technology innovation, it has been a common challenge on LGA devices the criticality of wirebonding process [5-7]. Wirebonding is defined as the process making electrical interconnection between the semiconductor die and the I/O leads using bonding wires.

For the device in focus, two different programs in one die for wirebonding is required with the first wire group having 0.6 mil wire size and same as the second wire group. During wirebonding process, shorting wire to its die occur as shown in Fig. 1.

2. METHODS, RESULTS & DISCUSSION

Important to note that it is crucial in wirebonding to eliminate or minimize “pigtail” on ball formation and have large bump on top surface. Fig. 2 shares a graphical analysis using a statistical tool. By using the tool, we have successfully defined a suitable bump parameter as seen in Fig. 3.

Staggered bond placement was evaluated to provide cap to wire clearance, 1st 2 wires offset +y; affected wire as is; 4th wire offset –y > single wire grouping > cap offset parameter not bond placement. Fig. 4 shows the comparison of the staggered bond placement evaluation.

The last kink (0.5 to 2 mils) was also evaluated to provide more clearance between wire and die. Fig. 5 shows the optimized last kink length to 0.5 mil.

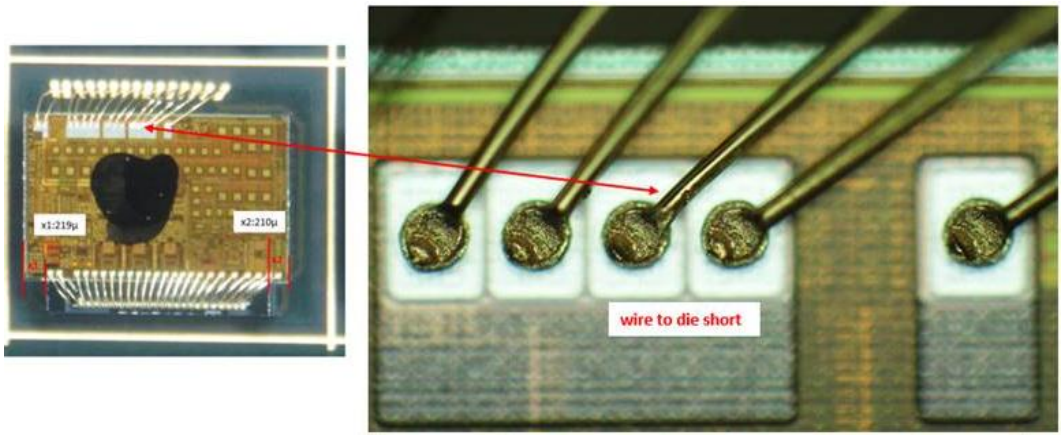

Fig. 1. One random wire on this group has wire to die shorting defect

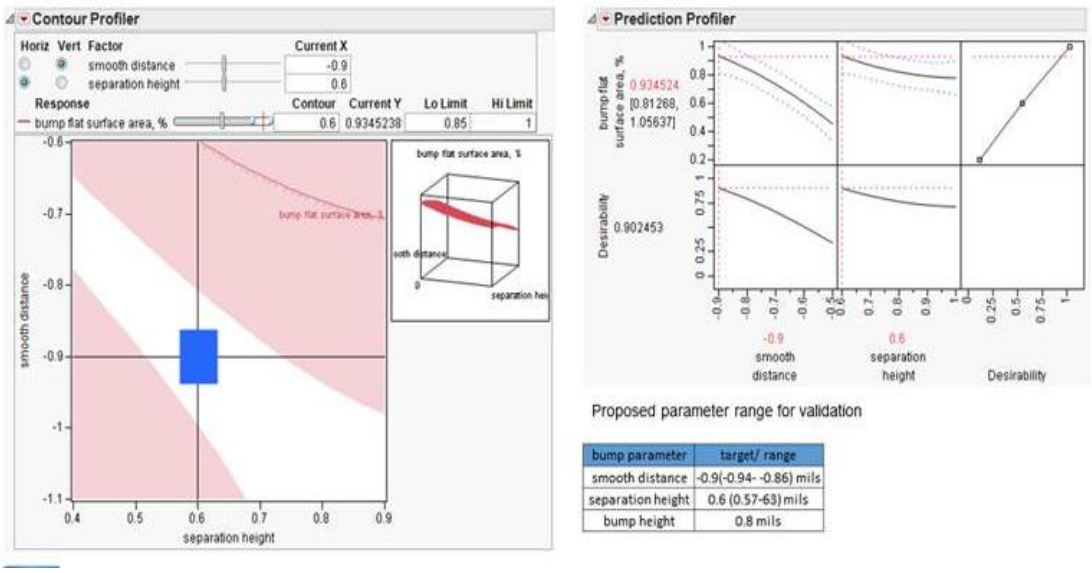

Fig. 2. Better parameters for bump ball to have larger size result

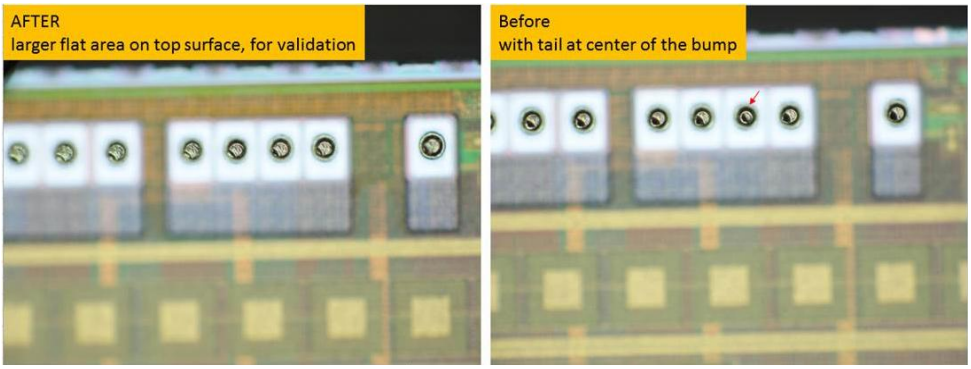

Fig. 3. Before and after effect of optimized ball parameters

Before After

Fig. 4. Before and after of ball placement correction

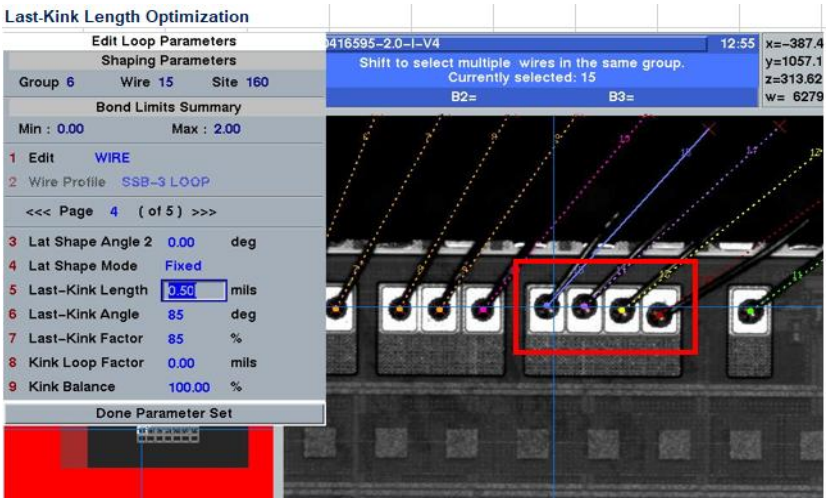

Fig. 5. Optimized last kink length to have more gap clearance on wire and die

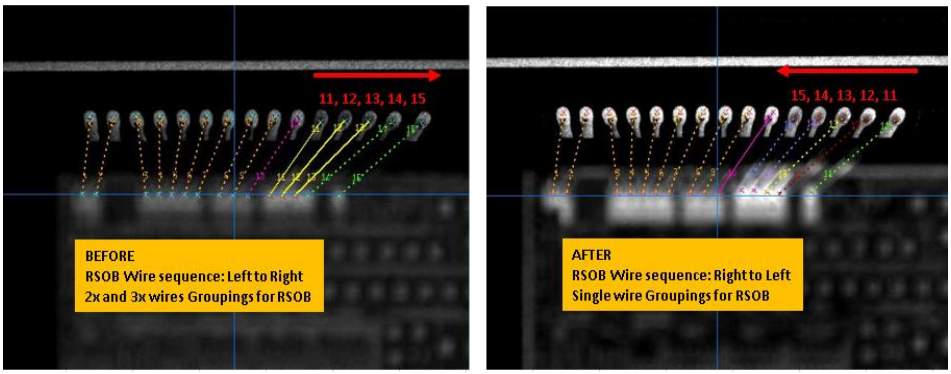

Fig. 6. Wire sequence was modified going from right to left on the affected group

Resequencing of reverse stitch on ball (RSOB) wires from was done as depicted in Fig. 6. The new sequence would prevent the capillary to hit wire shoulder on its loop.

Worthy to note that adjusting loop parameter and bond placement are critical, such that after adjusting the parameter, visual inspection was done on the unit. This was done to check the actual wirebonding result for possible wire to wire issue and found none. Loop height measurement also passed the requirement.

3. CONCLUSION AND RECOMMENDATIONS

With the wirebond process optimization through the adjustment in the looping parameter, bond placement and bonding sequencing can resolve shorting wires on substrate LGA device having two wire groups on a single line. With this, a flawless wirebonding operation was the result. For future works, the enhanced wirebonding solution could be applied on semiconductor devices with similar configuration. Also, works and learnings discussed in [8-12] are helpful to further improve the assembly processes focused on the wirebonding process.

DISCLAIMER

The product name used for this research is commonly and predominantly selected in our area of research and country. There is absolutely no conflict of interest between the authors and the company because we do not intend to use this company as an avenue for any litigation but for the advancement of knowledge.

ACKNOWLEDGMENT

The authors would like to express sincerest gratitude to the New Product Development & Introduction (NPD-I) team, Operations 1 Assembly Line Sustaining team, and the Management Team (MT) for the unwavering support provided.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Tsukada Y, et al. Trend of semiconductor packaging, high density and low cost. Proceedings of the 4th International Symposium on Electronic Materials and Packaging. Taiwan. 2002;1-6.
2. Yeap LL. Meeting the assembly challenges in new semiconductor packaging trend. 34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT). Malaysia. 2010;1-5.
3. Liu Y, et al. Trends of power electronic packaging and modeling. 10th Electronics Packaging Technology Conference. Singapore;2008.
4. Saha S. Emerging business trends in the semiconductor industry. Proceedings of PICMET '13: Technology Management in the IT-Driven Services (PICMET). USA. 2013;2744-2748.
5. Tan CE, et al. Challenges of ultimate ultra-fine pitch process with gold wire & copper wire in QFN packages. 36th International Electronics Manufacturing Technology Conference. Malaysia. 2014;1-5.
6. Ling J, et al. Wire bond reliability – an overview on the mechanism of formation/growth of intermetallics. Semicon. Singapore. 2008.
7. Tran TA, et al. Fine pitch probing and wirebonding and reliability of aluminum capped copper bond pads. IEEE 50th Electronic Components and Technology Conference (ECTC). USA. 2000;1674-1680.
8. Sumagpang Jr. A, et al. Package design improvement for wire shorting resolution. Journal of Engineering Research and Reports. 2020;11(2);41-44.
9. Descartin M, et al. Non-continuous IMC in copper wirebonding: key factor affecting the reliability. 6th International Conference on Electronic Packaging Technology (ICEPT). China. 2015;403-407.
10. Angeles A, Arellano IH. Understanding non-stick on lead wirebond failure due to leadfinger surface roughness. International Research Journal of Advanced Engineering and Science. 2019;4(2);49-54.
11. Sameoto D, et al. Wirebonding characterization and optimization on thick film su-8 mems structures and actuators. TRANSDUCERS 2007 - 2007 International Solid-State Sensors, Actuators and Microsystems Conference. France. 2007;2055-2058.
12. Moreno A, et al. Enhanced loop height optimization for complex configuration on

QFN device. 22nd IEEE Electronics Packaging Technology Conference (EPTC). Singapore. 2020;182-184.

Peer-review history:
The peer review history for this paper can be accessed here:
https://www.sdiarticle4.com/review-history/70393